Digital Charge Balance Controller with an Auxiliary Circuit for Superior Unloading Transient Performance of Buck Converters

Eric Meyer, Dong Wang, Liang Jia, Yan-Fei Liu
Department of Electrical & Computer Engineering
Queen's University
Kingston, Ontario, Canada
eric.meyer@amd.com, dong.wang@queensu.ca, liang.jia@queensu.ca, yanfei.liu@queensu.ca

***Abstract*— In this paper, a digital charge balance controller is presented which is capable of controlling a Buck converter and an auxiliary circuit to achieve an excellent unloading transient response. The auxiliary circuit significantly reduces the voltage overshoot caused by an unloading transient while the digital charge balance controller reduces the settling time of the converter. The controller is capable of implementing load-line regulation and yields a smooth transition from one loading condition to another. Simulation and experimental verification is performed and demonstrates significant transient improvement over previously-proposed solutions.**

I. INTRODUCTION

As the capabilities of high-performance digital devices continue to exponentially expand, the demand on the power electronics industry to supply such devices becomes increasingly complex. Load transients of digital devices are becoming larger while physical real-estate constraints are becoming tighter preventing the tried-and-true method of adding capacitors to improve the transient performance of Buck converters. Thus, extensive research has been conducted developing controllers which improve the transient performance of Buck converters to their physical limits.

In [1]-[11], controllers have been presented which utilize second-order sliding surfaces, pre-calculated switching time intervals or capacitor charge balance methodologies to reduce the voltage deviation and settling time of a Buck converter, undergoing a load transient, to its virtually optimal level.

However ,it is demonstrated in [1]-[2] that for low duty cycle conversion applications (e.g. 12VDC→1.5VDC), the optimal voltage overshoot caused by a step-down load current transient may be more than 5 times as large as the corresponding voltage undershoot caused by a positive current step of equal magnitude, as illustrated in Figure 1. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition.

Thus in [12]-[22], various auxiliary circuits for the Buck converter have been proposed to improve the transient performance of a converter undergoing high-to-low load

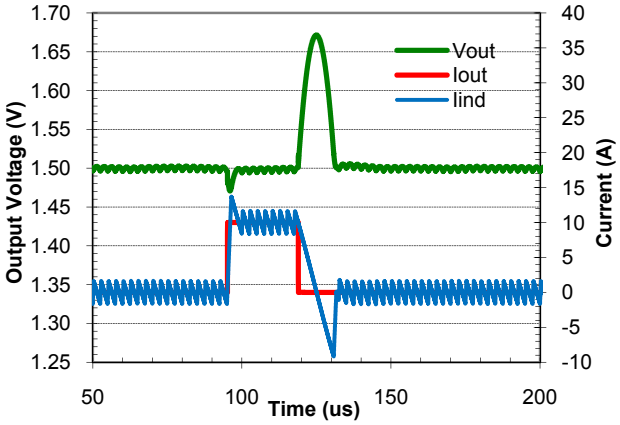

Figure 1 Assymetrical transient response to positive/negative load current step change (charge balance controller response)

current changes. Methods include temporarily inversing the converter's input voltage, temporarily disconnecting the inductor from the load, or diverting a portion of the inductor current to the input of the Buck converter through a separate switching circuit.

For example, the unloading transient response is improved in [12] by utilizing the high-frequency switching auxiliary circuit (illustrated in Figure 2) which rapidly transfers current from the output of the Buck converter to its input.

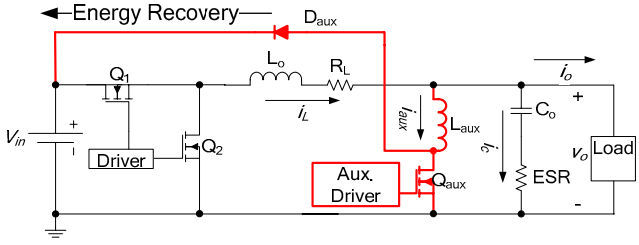

Figure 2 Implementaiton of high frequency auxiliary circuit

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While such methods do improve the unloading transient performance of a Buck converter, there has been no attempt to simultaneously reduce the voltage overshoot *and* minimize the settling time through control methods such as those presented in [1]-[11]. As an example, Figure 3 shows a simulated comparison of the unloading transient response of the non-linear charge balance controller (presented in [1]-[2]), versus the auxiliary circuit and control method, presented in [12].

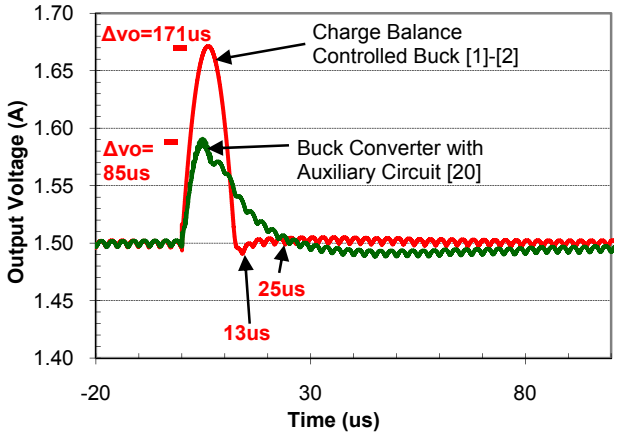

Figure 3 Charge Balance Control Respone [1]-[2] vs. Auxiliary Circuit Response [20]

It is shown in Figure 3 that while the addition of the aforementioned auxiliary circuit significantly reduces the voltage overshoot caused by an unloading transient, the settling time of the charge balance controller is far superior.

Furthermore, previously-proposed methods do not address applications in which load-line regulation (a.k.a. adaptive voltage positioning AVP) is required.

In this paper, a digital charge balance controller is proposed which combines the auxiliary circuit, presented in [12] and illustrated in Figure 2, with the control methodology presented in [1]-[2] to yield a converter with superior unloading transient performance. The proposed method actively reduces the output voltage overshoot caused by an unloading transient while minimizing the settling time to virtually-optimal levels (an achievement not demonstrated in previous literature).

Since the detailed implementation of the auxiliary circuit is covered extensively in [12], this paper will focus primarily on the proposed modified charge balance control method.

II. Concept of Operation

The operation of the proposed method will be described without and with the use of load-line regulation.

A. Operation without Load-Line Regulation

Figure 4 illustrates the proposed controller's reaction to a rapid unloading transient without load-line regulation.

The high-level operation can be described in 5 steps:

1. The converter is controlled by a linear voltage-mode control scheme during steady-state conditions.
2. Immediately following an unloading transient, the controller will set the Buck converter's PWM signal low and set the auxiliary circuit's PWM signal high.

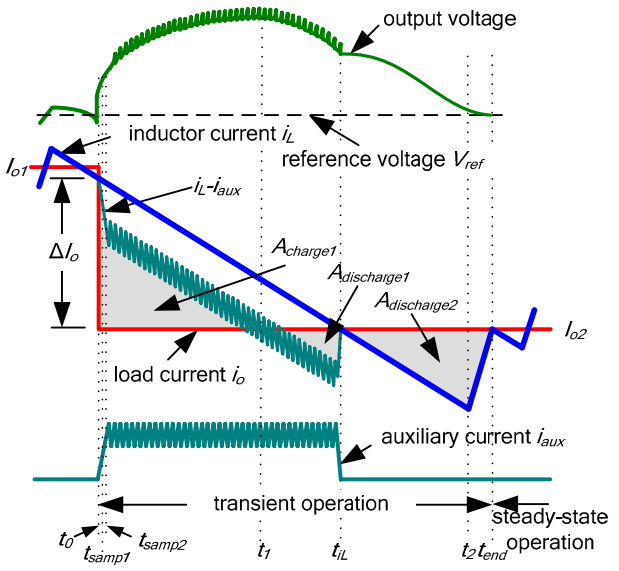

Figure 4 Proposed controller reaction to an unloading transient (w/o load-line regulation)

3. The controller will estimate the magnitude of the unloading transient $|\Delta I_o|$ and set the peak auxiliary current I_{aux_peak} to an appropriate level based on $|\Delta I_o|$. At this point, the auxiliary circuit will begin switching operation, transferring current from the Buck converter's output to its input.
4. At the moment that the inductor current i_L first equals the new load current I_{o2} (at t_{iL}), the auxiliary circuit will be deactivated. However, the Buck converter's PWM signal will continue to remain low.
5. The Buck converter's PWM signal will be set high at t_2 causing the inductor current to increase toward I_{o2}. t_2 should be such that the net capacitor charge is equal to zero at the exact moment that the inductor current equals the new load current for a second time. In other words, referring to Figure 4, $A_{charge1} = A_{discharge1} + A_{discharge2}$ when $i_L = I_{o2}$ at t_{end}. This will ensure that the output voltage and the inductor current equal their respective steady-state values simultaneously at t_{end}.

B. Operation with Load-Line Regulation

Two cases must be addressed when charge balance control, the auxiliary circuit and load-line regulation are employed.

1) Case #1 ($v_o > V_{o2}$ when $i_L = I_{o2}$)

Case #1 is illustrated in Figure 5.

As shown, after the moment that i_L first equals I_{o2} ($t \geq t_{iL}$), additional charge must be removed from the capacitor such that the output voltage can decrease to its new steady-voltage V_{o2}. Therefore, the PWM control signal will remain low until t_2. t_2 is such that the charge balance equation (1) is true.

$$A_{charge1} - A_{discharge1} - A_{discharge2} = \int_{t_0}^{t_1} (i_L - i_{aux} - i_o)\,dt - \int_{t_1}^{t_{iL}} (i_o - i_{aux} - i_L)\,dt - \int_{t_{iL}}^{t_2} (i_o - i_L)\,dt = (I_{o1} - I_{o2}) \cdot R_{droop} \cdot C_o \quad (1)$$

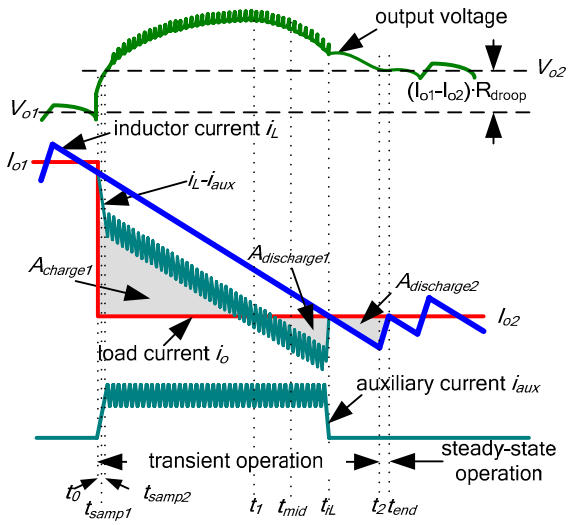

Figure 5 Controller reaction to an unloading transient with load-line regulation (Case #1)

Where $A_{charge1}$, $A_{discharge1}$, $A_{discharge2}$ are the capacitor current integral areas shown in Figure 5.

2) Case #2 ($v_o = V_{o2}$ before $i_L = I_{o2}$)

Case #2 is shown in Figure 6.

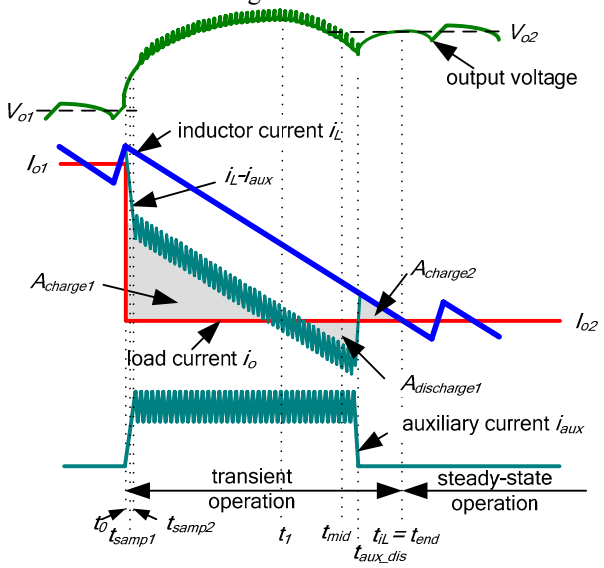

Figure 6 Controller reaction to an unloading transient with load-line regulation (Case #2)

As shown, during Case #2, the output voltage v_o equals its new steady-state voltage V_{o2} before i_L equals I_{o2}. In this case, the auxiliary circuit will be de-activated *prior* to i_L equalling I_{o2} (at t_{aux_dis}). t_{aux_dis} will be such that equation (2) is satisfied.

$$A_{charge1} - A_{discharge1} + A_{charge2} = \int_{t_0}^{t_1} (i_L - i_{aux} - i_o)\,dt - \int_{t_1}^{t_{aux\_dis}} (i_o - i_{aux} - i_L)\,dt + \int_{t_{aux\_dis}}^{t_{end}} (i_L - i_o)\,dt = (I_{o1} - I_{o2}) \cdot R_{droop} \cdot C_o \quad (2)$$

The Buck converter's PWM signal will be held low until the inductor current equals the new load current (at t_{iL}). At this point, the linear controller will retain control.

III. Mathematical Analysis of Charge Balance Controller with Auxiliary Circuit

This section will derive the charge balance equations necessary to implement digital charge balance control such that a Buck converter, with the proposed auxiliary circuit, will recover from an unloading transient with decreased settling time. The charge balance equations are presented without and with load-line regulation employed.

A. Without Load-Line Regulation

Referring to Figure 4, it is noted that there is one positive integral area of capacitor current $A_{charge1}$ and two negative integral areas of capacitor current $A_{discharge1}$ and $A_{discharge2}$. The capacitor charge area $A_{charge1}$ is derived in (3).

$$A_{charge1} = \iint_{t_0}^{t_1} m_2\,dtdt \quad (3)$$

m_2 is the falling slew rate of the inductor current i_L ($m_2 \approx V_o/L_o$). t_1 represents the first moment that the capacitor current i_c equals zero (i.e. when i_L-I_{aux_avg}=I_{o2}).

Referring to Figure 4, it is shown that the auxiliary circuit is de-activated when the inductor current equals the new load current (at t_{iL}). It is assumed that when the auxiliary circuit is de-activated, that the auxiliary current i_{aux} decreases to zero in negligible time. This is a fair assumption since the falling i_{aux} slew rate is much faster than the falling i_L slew rate.

For the charge balance equations, the ripple of the auxiliary current is neglected since the high frequency auxiliary switching causes the ripple's effect to be neutralized.

With the above assumptions, $A_{discharge1}$ is calculated in (4).

$$A_{discharge1} = \iint_{t_1}^{t_{iL}} m_2\,dtdt \quad (4)$$

Through geometric observation and simplification, $A_{discharge2}$ is expressed in (5).

$$A_{discharge2} = \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1}\,dtdt \quad (5)$$

m_1 is the rising slew rate of the inductor current i_L ($m_1 \approx (V_{in}-V_o)/L_o$). In order to ensure that v_o and i_L equal their respective steady-state values simultaneously, the net capacitor charge over the transient period must equal zero, as expressed in (6).

$$A_{charge1} - A_{discharge1} - A_{discharge2} = 0$$
$$\iint_{t_0}^{t_1} m_2\,dtdt - \iint_{t_1}^{t_{iL}} m_2\,dtdt - \iint_{t_{iL}}^{t_2} \frac{m_1 \cdot m_2 + m_2^2}{m_1}\,dtdt = 0 \quad (6)$$

By dividing both sides of (6) by the constant m_2 and substituting the known values for m_1 and m_2, multiplying both sides by (V_{in}-V_o) and simplifying, equation (7) is created.

$$(V_{in} - V_o) \cdot \iint_{t_0}^{t_1} dt\,dt - (V_{in} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\,dt - V_{in} \cdot \iint_{t_{iL}}^{t_2} dt\,dt = 0 \quad (7)$$

Therefore, by using (7), it is possible to determine the moment that the Buck converter's PWM control signal should be set high (at t_2), by the use of two accumulators, connected in series. The waveforms of the double accumulator are shown in Figure 6. This methodology is similar to the double accumulator method presented in [2].

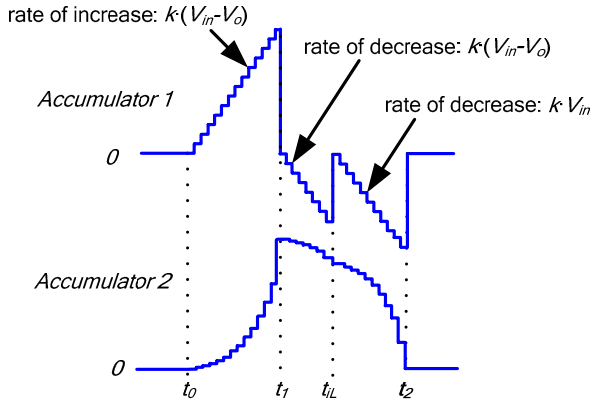

Figure 7 Digital double accumulator to determine t_2 without load-line regulation

As shown, when the output of *accumulator 2* returns to zero, t_2 is determined and the Buck converter's PWM signal is set high. This control strategy is suitable when load-line regulation is not employed; however, it must be modified when load-line regulation is employed.

B. With Load-Line Regulation

This subsection will be divided into Case #1 and Case #2, as previously described in Section II.

1) Case #1 ($v_o > V_{o2}$ when $i_L = I_{o2}$)

The capacitor charge regions for Case #1 are illustrated in Figure 5. As shown, a time instant t_{mid} has been identified in Figure 5. t_{mid} will be used in the charge balance calculation and occurs when (8) is true.

$$i_L - I_{o2} = \frac{1}{2} \cdot I_{aux_{avg}} \quad when\ t = t_{mid} \tag{8}$$

As shown, t_{mid} bisects time instants t_1 and t_{iL}. The use of t_{mid} will be discussed in this section. The method of detecting t_{mid} will be discussed in Section IV.

The charge balance equation can be obtained by modifying (7), as expressed in (8).

$$(V_{in} - V_o) \cdot \iint_{t_0}^{t_1} dt\,dt - (V_{in} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\,dt - V_{in} \cdot \iint_{t_{iL}}^{t_2} dt\,dt = (V_{in} - V_o) \cdot R_{droop} \cdot C_o \cdot \int_{t_0}^{t_{iL}} dt \tag{9}$$

The right side of equation (9) represents the required capacitor charge offset to implement load-line regulation. As expressed, the output of an additional accumulator (the *load-line accumulator*) is compared with the output of the double accumulator to determine t_2.

Since t_{mid} bisects time instances t_1 and t_{iL} and the input of the *load-line accumulator* is a constant, the final value of the *load-line accumulator* is obtained at time instant t_{mid}, as expressed in (10).

$$\int_{t_0}^{t_{iL}} dt = \int_{t_0}^{t_1} dt + \int_{t_1}^{t_{mid}} dt + \int_{t_{mid}}^{t_{iL}} dt = \int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{mid}} dt \tag{10}$$

By substituting (10) into (9), the charge balance equation for load-line regulation (Case #1) is derived in (11).

$$(V_{in} - V_o) \cdot \iint_{t_0}^{t_1} dt\,dt - (V_{in} - V_o) \cdot \iint_{t_1}^{t_{iL}} dt\,dt - V_{in} \cdot \iint_{t_{iL}}^{t_2} dt\,dt = (V_{in} - V_o) \cdot R_{droop} \cdot C_o \cdot \left(\int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{mid}} dt \right) \tag{11}$$

Thus, t_2 can be determined by using the aforementioned double accumulator (left side of (11)) and comparing its output with the output of a single accumulator (right side of (11)).

2) Case #2 ($v_o = V_{o2}$ before $i_L = I_{o2}$)

The capacitor charge regions for Case #2 are illustrated in Figure 6. It is shown that, for Case #2, the moment the auxiliary circuit is de-activated t_{aux_dis} occurs before t_{iL} to allow charge area $A_{charge2}$ to charge the output capacitor.

If the auxiliary circuit were de-activated at t_{mid}, the capacitor current (i_L-I_{o2}) would equal I_{o2}+I_{aux_avg}, which can also be expressed in terms of the falling inductor slew rate, as shown in (12).

$$i_L(t_{mid}) - I_{o2} = \int_{t_1}^{t_{mid}} m_2 dt \tag{12}$$

Following t_{mid}, the charge area $A_{charge2}$ begins to decrease as the inductor current approaches the new load current at a slew rate of m_2. Thus, $A_{charge2}$ is expressed in (13).

$$A_{charge2} = A_{discharge1} - \int_{t_{mid}}^{t_{aux\_dis}} \left(i_L(t_{mid}) - I_{o2} - m_2 \cdot \int_{t_{mid}}^{t_{aux\_dis}} dt \right) d\tau \tag{13}$$

By substituting (3),(4),(10),(13), into (2), the charge balance equation for Case #2 load line regulation is expressed in (14).

$$\iint_{t_0}^{t_1} m_2\,dt dt - \iint_{t_1}^{t_{aux\_dis}} m_2\,dt dt + \iint_{t_1}^{t_{mid}} m_2 dt\,dt - \int_{t_{mid}}^{t_{aux\_dis}} \left(\int_{t_1}^{t_{mid}} m_2 dt - \int_{t_{mid}}^{t_{aux\_dis}} m_2 dt \right) d\tau = R_{droop} \cdot C_o \cdot \left(\int_{t_0}^{t_1} m_2 dt + 2 \cdot \int_{t_1}^{t_{mid}} m_2 dt \right) \tag{14}$$

By collecting like terms, (14) is simplified, as shown in (15).

$$\iint_{t_0}^{t_1} dt\,dt - \int_{t_{mid}}^{t_{aux\_dis}} \left(2 \cdot \int_{t_1}^{t_{mid}} dt \right) dt = R_{droop} \cdot C_o \cdot \left(\int_{t_0}^{t_1} dt + 2 \cdot \int_{t_1}^{t_{mid}} dt \right) \tag{15}$$

By using (15), the output of a double accumulator (left side) can be compared to the output of a single accumulator (right side) to determine the moment to deactivate the auxiliary circuit t_{aux_dis}.

In order to minimize the digital gate count of the controller, it is beneficial to design one double accumulator that can be used for Case #1, Case #2 and cases without load-line regulation. In order to achieve this, charge balance equation (15) can be modified by multiplying both sides by (V_{in}-V_o), as expressed in (16).

$$(V_{in}-V_o)\cdot\iint_{t_0}^{t_1} dt\,dt-(V_{in}-V_o)\cdot\int_{t_{mid}}^{t_{aux\_dis}}\left(2\cdot\int_{t_1}^{t_{mid}} dt\right)d\tau$$
$$=R_{droop}\cdot C_o\cdot(V_{in}-V_o)\cdot\left(\int_{t_0}^{t_1} dt+2\cdot\int_{t_1}^{t_{mid}} dt\right) \quad (16)$$

By utilizing the combination of (11) and (16), one double accumulator can be used for all cases, as shown in Figure 8.

Figure 8 illustrates the load-line accumulator output for Case #2, Case #1 and no load-line (from top to bottom).

As shown, if the output of *accumulator 2* decreases below that of the *load-line accumulator* before t_{iL}, Case #2 is detected and the auxiliary circuit is de-activated, at time t_{aux_dis}.

If t_{iL} occurs before the output of *accumulator 2* decreases below the output of the *load-line accumulator*, the auxiliary circuit is de-activated at t_{iL}, as shown in Figure 4 and Figure 5. In these cases, the Buck converter's PWM signal will remain low until output of *accumulator 2* decreases below the *load-line accumulator*'s output at time t_2.

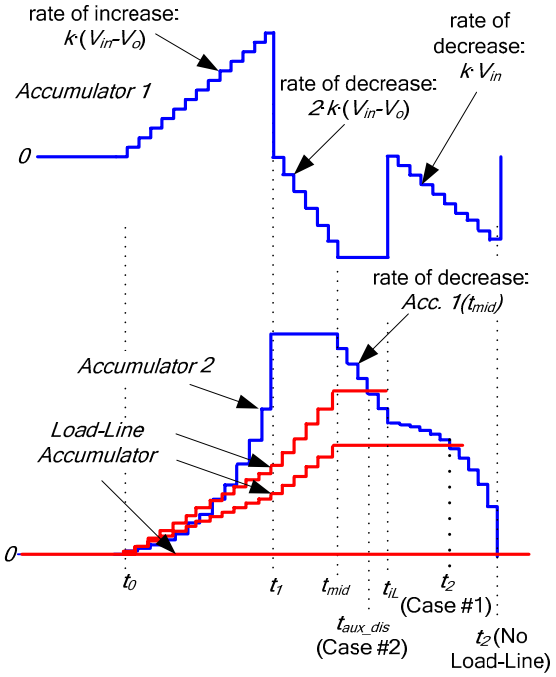

Figure 8 Digital double for all possible cases

IV. Detailed Operation and Implementation of Charge Balance Controller with Auxiliary Circuit

The high-level system diagram of the digital charge balance controller with auxiliary circuit for a synchronous Buck converter is illustrated in Figure 9.

This section summarizes the operation of the proposed charge balance controller with the auxiliary circuit. The operation of the controller can be summarized in eight steps.

Step 1 ($t=t_0$)

The Buck converter is controlled by a digital linear controller during steady-state operation. Following an unloading transient, the output of the analog load transient detector (see Figure 9) will rapidly exceed the transient threshold.

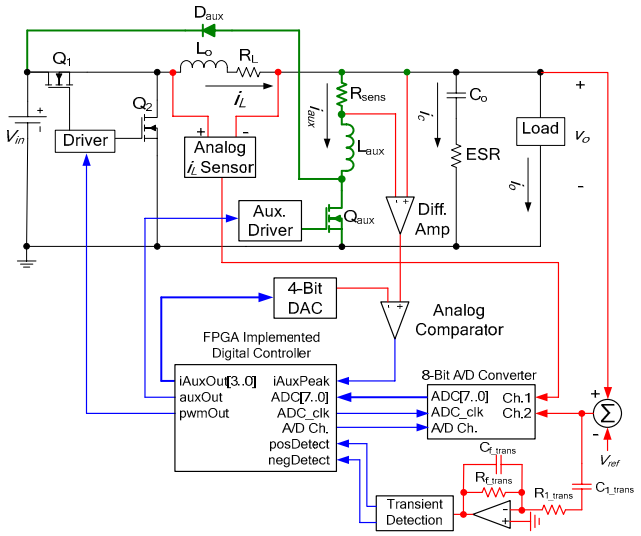

Figure 9 System-level block diagram of digitally-implemented charge balance controller with auxiliary circuit

This will cause the controller to immediately enter transient mode. The linear controller will be frozen and the charge balance controller will take control of the converter.

The PWM signal of the Buck converter will be initially set low and the PWM signal of the auxiliary circuit will be initially set high.

As shown in Figure 8, the output of *accumulator 1* will begin to increase linearly with a slope of $k\cdot(V_{in}-V_o)$ and the output of *accumulator 2* will begin to increase exponentially. If load-line regulation is required, the *load-line accumulator* will begin to increase linearly with a slope of $k^2\cdot R_{droop}\cdot C_o\cdot(V_{in}-V_o)$.

Step 2 ($t_{samp1}\le t\le t_{samp2}$)

As shown in Figure 4-Figure 6, two output voltage samples are acquired at t_{samp1} and t_{samp2} to estimate the load transient magnitude. Using this information and equation (17), an appropriate value of I_{aux_peak} is selected from an LUT. The digital value I_{aux_peak} is passed to the system's DAC and the i_c cross-over predictor. At t_{samp2}, the auxiliary circuit will begin high-frequency switching operation using a peak-current, constant off-time controller. The appropriate peak current is user defined based on the desired output voltage response.

$$\Delta I_o=C_o\cdot\frac{\Delta v_{o\_samp}}{T_{samp}}+\left[V_o\cdot\left(\frac{1}{L_{aux}}+\frac{1}{L_o}\right)\cdot\left(t_{samp2}-{}^1\!/_2\cdot T_{samp}-t_0\right)+ESR\right] \quad (17)$$

It is shown in Figure 9, that an analog comparator is used to detect the peak auxiliary current I_{aux_peak}. The detection signal is used by the digital controller. The mixed-signal implementation is necessary due to the high slew rate of the auxiliary current.

Step 3 ($t=t_1$)

The capacitor current crosses zero for the first time at t_1. In order to predict the time instances t_1, t_{mid} and t_{iL}, a capacitor current zero cross-over predictor is utilized. This method is introduced in [2]; however in the proposed method, the predictor is capable of compensating for the known average auxiliary current I_{aux_avg}. The predictor acquires output voltage

samples (at a frequency equivalent to auxiliary circuit switching frequency f_{aux}) for a short period after t_0. From these samples, it is possible to calculate the derivative, estimate the capacitor current slope and magnitude allowing for the fine resolution prediction of t_1, t_{mid} and t_{iL}, as shown in Figure 10.

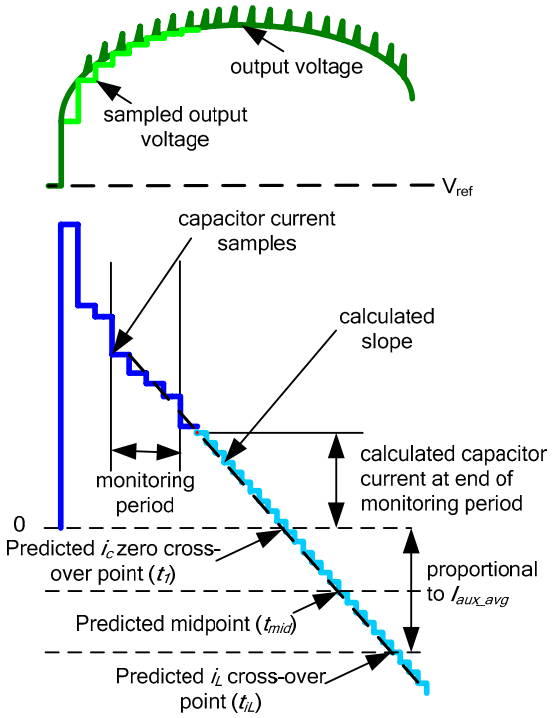

Figure 10 Prediction of t_1, t_{mid} and t_{iL} by capacitor current zero cross-over predictor

Referring to Figure 8, at t_1, *accumulator 1* is reset to zero. The input of *accumulator 1* is set to $-2\cdot(V_{in}-V_o)$ and the enable input of *accumulator 2* is set low. Thus, the output of *accumulator 1* will begin to decrease at a rate of $2\cdot k\cdot(V_{in}-V_o)$ and the output of *accumulator 2* will remain constant.

The channel select of the ADC is set to the inductor current sensor at this point, and a sample of the inductor current is taken and passed to the linear controller. This will be used by the linear controller for load-line regulation.

Referring to Figure 8, the input of the *load-line accumulator* is switched to $2\cdot k\cdot R_{droop}\cdot C_o\cdot(V_{in}-V_o)$ at t_1.

Step 4 ($t=t_{mid}$)

When the i_c zero cross-over predictor indicates $t=t_{mid}$, it is known that $i_L-I_{o2}=\frac{1}{2}\cdot I_{aux\_avg}$. Referring to Figure 8, at $t=t_{mid}$, the *enable* input of *accumulator 1* is set low and the enable input of *accumulator 2* is set high. *Accumulator 2* is set to decrement mode causing its output to decrease at a linear rate equal to $k\cdot Acc1(t_{mid})$ (where $Acc1(t_{mid})$ equals the output of *accumulator 1* at $t=t_{mid}$).

As shown in Figure 8, the enable input of the *load-line accumulator* is set low at t_{mid}, causing its input to remain constant following t_{mid}.

Step 5 ($t=t_{aux\_dis}$) (Case #2 only)

As shown in Figure 8, if the output of *accumulator 2* decreases below that of the *load-line accumulator* before the inductor current equals the new load current (at t_{iL}) then Case #2 is detected. If this occurs, the auxiliary circuit is de-activated at this moment ($t=t_{aux\_dis}$), as shown in Figure 6. The PWM signal of the Buck converter continues to be held low.

Step 6 ($t=t_{iL}$)

When the inductor current equals the new load current for the first time, $t=t_{iL}$.

If Case #2 was previously detected, this moment signifies the end of the load transient and the linear controller re-takes control of the Buck converter.

If Case #2 was not previously detected, *accumulator 1* is cleared and its input is switched to $-V_{in}$. This causes *accumulator 1*'s output to decrease at a rate of $k\cdot V_{in}$ and the output of *accumulator 2* to decrease at an exponential rate. As shown in Figure 4 and Figure 5, the auxiliary circuit is de-activated and the PWM control signal is held low following t_{iL}.

Step 7 ($t=t_2$) (No Load-Line Regulation or Case #1)

When the output of *accumulator 2* decreases below that of the *load-line accumulator* (at t_2), the PWM signal of the Buck converter is switched high and the inductor current begins to increase toward the new load current, as shown in Figure 4 and Figure 5.

Step 8 ($t=t_{end}$)

When the inductor current equals the new load current for the first time (for Case #2) or the inductor current equals the new load current for a second time, it is determined that the transient is over. The second current cross-over is detected using a digital accumulator (*accumulator 3*), as introduced in [2]. The linear controller is unfrozen and retakes control of the Buck converter.

V. Simulation Results

The following simulation was conducted under the ideal case, without considering timing delays, digital quantization effects, etc. The purpose of the simulation was to demonstrate the effectiveness of the charge balance controller with the auxiliary circuit over (1) a linear analog controller and (2) the charge balance controller alone.

The parameters of the simulated Buck converter were as follows: V_{in}=12V, V_o=1.5V, f_{sw}=400kHz, L_o=1uH, C_o=180uF, ESR=0.5mΩ, ESL=100pH. The auxiliary circuit parameters were: L_{aux}=100nH, $f_{aux}\approx$2MHz.

The transient response was simulated with load-line regulation. The output impedance R_{droop} was set to 5mΩ. Figure 11 illustrates a simulated comparison between a voltage-mode controlled converter, a digital charge balance controlled Buck converter (without auxiliary circuit) [2] and the proposed digital charge balance controller with auxiliary circuit. Each converter undergoes a 10A→0A load step transient.

It is illustrated that the voltage deviation magnitude and the settling time is improved significantly over previously-proposed solutions. The Buck converter with the proposed controller and auxiliary circuit has an output voltage overshoot of 18 mV (68mV-50mV) over the new steady-state voltage (68mV over the original steady-state voltage) and a settling time of 7us.

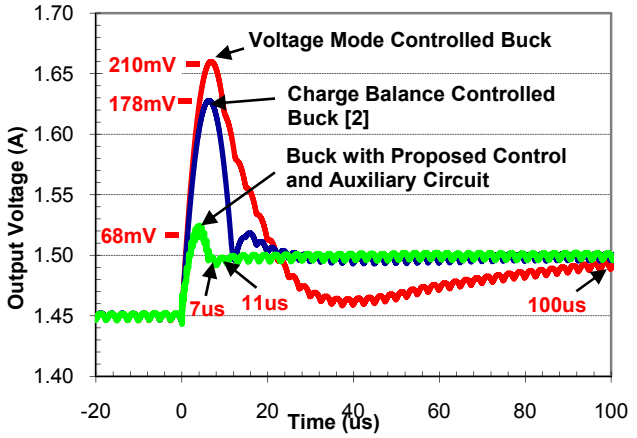

Figure 11 Simulated response to a 10A→0A load current step change with load line regulation (I_{aux_avg} = 3.8A)

VI. Experimental Results

The proposed controller was implemented on an Altera Cyclone II FPGA. The Buck converter and auxiliary circuit parameters were identical to those of the simulation.

Figure 12 illustrates the controller's reaction to an 11.5A→0A load step (without load line regulation). For this unloading magnitude, the auxiliary current was set to approximately I_{aux_avg}=3.5A. For reference, the time instants t_0-t_{end} were super-imposed on the scope display to better illustrate the controller's behavior.

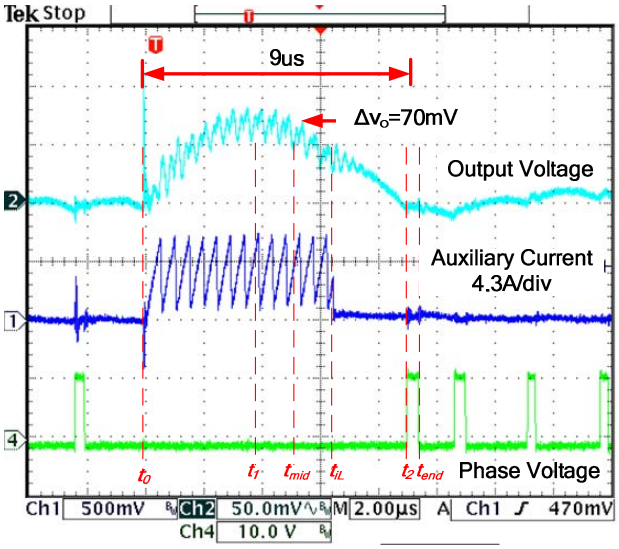

Figure 12 Digital charge balance controller's response to a 11.5A→0A load step without load line regulation

As shown in Figure 13, the auxiliary circuit is de-activated when the inductor current first equals the new load current (at t_{iL}). However, the Buck converter`s PWM signal is kept low until t_2 is determined. This is to allow additional charge to be removed from the output capacitor such that the output voltage equals the reference voltage at the exact moment that the inductor current equals its new steady-state value.

The converter is capable of recovering from the load transient within 9us with a voltage overshoot of 70mV.

Figure 13 illustrates the unloading transient response of the digital charge balance controller (introduced in [2]) without the use of the auxiliary circuit.

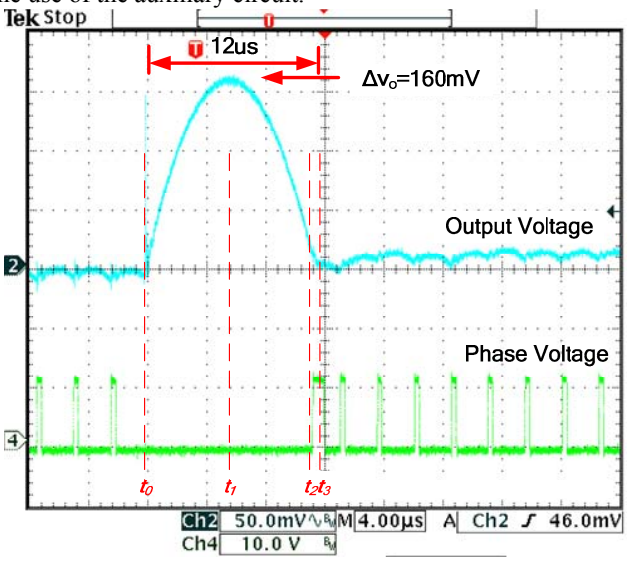

Figure 13 Digital charge balance controller's response (without auxiliary circuit) to a 11.5A→0A load step without load line regulation

As observed, the use of the auxiliary circuit improves the settling time by 25% (12us→9us) and improves the voltage overshoot by 56% (160mV→70mV) over that of the digital charge balance controller alone.

Figure 14 illustrates the controller's reaction to an 11.5A→0A load step (with load line regulation). Figure 15 illustrates the inductor current (measured from the analog inductor current sensor).

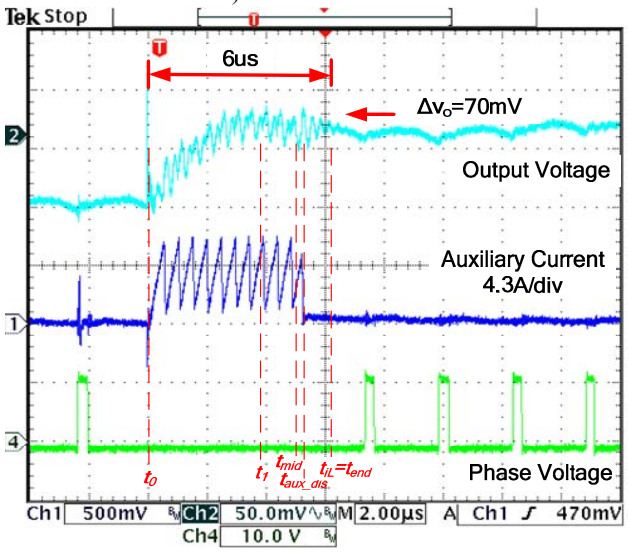

Figure 14 Digital charge balance controller's response to an 11.5A→0A load step with load line regulation

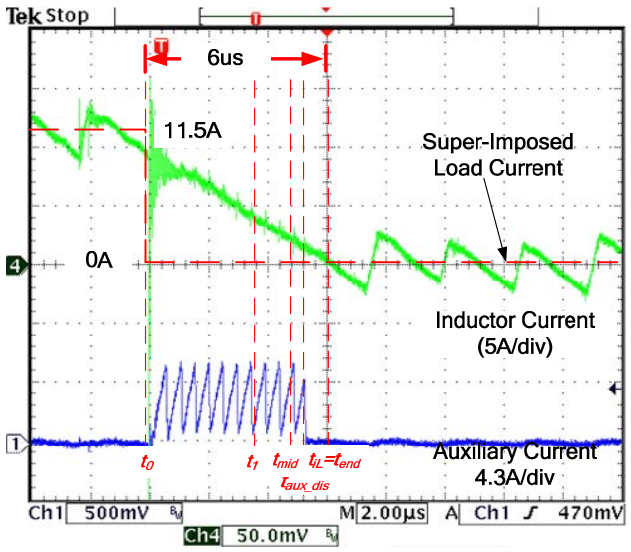

Figure 15 Digital charge balance controller's response to an 11.5A→0A load step with load line regulation (inductor current and auxiliary current)

As illustrated, Case #2 occurs and the auxiliary circuit is deactivated before t_{iL}. The auxiliary current is deactivated at t_{aux_dis} to allow the capacitor charge areas to appropriately balance by time t_{iL}. This results in a smooth transition as the output voltage equals its new steady-state value at the exact moment that the inductor current equals the new load current. The converter is able to recover from the unloading step within 6us and with only a 10mV (70mV-60mV) overshoot beyond the final steady-state voltage.

VII. Conclusions

In this chapter a novel digital charge balance control method is described capable of reducing the voltage overshoot of a Buck converter (through the use of an auxiliary circuit) *and* implementing load line regulation. The proposed digital controller does not require multipliers, dividers or two-dimensional LUTs, significantly reducing the IC real-estate required.

The use of the auxiliary circuit significantly reduces the voltage overshoot (due to an unloading transient) beyond the physical capabilities of the Buck converter alone. It is shown that by implementing the charge balance principle with the auxiliary circuit, that the settling time can be also significantly improved over previously proposed solutions. In addition, it is demonstrated that the controller can be extended to applications which require load-line regulation.

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